Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A semiconductor device having a gate electrode formed on a semiconductor layer with a gate insulating film interposed therebetween and a source/drain formed in the semiconductor layer, said semiconductor layer being curved from a region directly below said gate electrode sandwiched by said source/drain toward a region near said source/drain.

[c2] 2. The semiconductor device according to claim 1, wherein said region directly below said gate electrode is strained by the curved semiconductor layer.

[c3] 3. The semiconductor device according to claim 1, wherein a cavity is defined below said source/drain formed in the semiconductor layer and below the region directly below said gate electrode sandwiched by said source/drain.

[c4] 4. The semiconductor device according to claim 1, wherein an insulating film is formed below said source/drain formed in the semiconductor layer and below the region directly below said gate electrode sandwiched by said source/drain.

[c5] 5. The semiconductor device according to claim 1, wherein said source/drain is of a stacked source/drain structure comprising another semiconductor layer formed on said semiconductor layer to provide a thick film and an impurity subsequently introduced into the thick film.

[c6] 6. A method of manufacturing a semiconductor device having a gate electrode formed on a semiconductor layer with a gate insulating film interposed therebetween and a source/drain formed in the semiconductor layer, comprising the steps of:
forming a laminated region of a sacrificial layer and a semiconductor layer and a device separating region surrounding said laminated region, on a substrate;
forming a gate electrode on said device separating region and said semiconductor layer with a gate insulating film interposed therebetween;
forming an opening through which said sacrificial layer is exposed between said device separating region and said semiconductor layer; and
removing said sacrificial layer through said opening to form a cavity below said semiconductor layer.

[c7] 7. The method according to claim 6, further comprising the step of:

after the step of removing said sacrificial layer through said opening to form the cavity below said semiconductor layer, curving said semiconductor layer.

[c8] 8. The method according to claim 6, wherein said step of forming the opening comprises the step of:
removing said device separating region toward said substrate to partly expose a side surface of said sacrificial layer thereby to form said opening.

[c9] 9. The method according to claim 6, wherein said step of forming the laminated region and the device separating region comprises the steps of:
forming said sacrificial layer and said semiconductor layer on said substrate to form said laminated region; and
thereafter, forming said device separating region surrounding said laminated region and extending to said substrate.

[c10] 10. The method according to claim 6, wherein said step of forming the laminated region and the separating region comprises the steps of:
forming said device separating region on said substrate so as to project from a surface of the substrate; and
thereafter, forming said sacrificial layer and said semiconductor layer on said substrate in a region surrounded

by said device separating region to form said laminated region.

[c11] 11. The method according to claim 7, wherein said step of curving said semiconductor layer comprises the step of:
curving said semiconductor layer under a surface tension acting between said semiconductor layer and said substrate.

[c12] 12. The method according to claim 7, further comprising the steps of:
after the step of forming the gate electrode, forming a thermally elongatable film on the entire surface, wherein after said thermally elongatable film is formed on the entire surface, said opening through which said sacrificial layer is exposed is formed between said device separating region and said semiconductor layer, and said sacrificial layer is removed through said opening to form said cavity below said semiconductor layer;
wherein said step of curving said semiconductor layer comprises the step of:
curving said semiconductor layer by heating said thermally elongatable film to thermally elongate said thermally elongatable film.

[c13] 13. The method according to claim 7, further comprising

the steps of:

after the step of forming the gate electrode, introducing ions into said semiconductor layer, wherein after the ions are introduced into said semiconductor layer, said opening through which said sacrificial layer is exposed is formed between said device separating region and said semiconductor layer, and said sacrificial layer is removed through said opening to form said cavity below said semiconductor layer;

wherein said step of curving said semiconductor layer comprises the step of:

curving said semiconductor layer by heating said semiconductor layer to curve said semiconductor layer.

[c14] 14. The method according to claim 6, wherein said sacrificial layer comprises a BOX layer of an SOI substrate, and said semiconductor layer comprises a thin-film semiconductor layer formed on an uppermost layer of said SOI substrate.

[c15] 15. The method according to claim 6, further comprising the steps of:

before or after the step of removing said sacrificial layer, forming a source/drain in said semiconductor layer in sandwiching relation to a region directly below said gate electrode; and

following said step of forming said source/drain, sili-

cidizing said source/drain entirely or partly.

[c16] 16. The method according to claim 6, further comprising the steps of:
before or after the step of removing said sacrificial layer, forming another semiconductor layer on said semiconductor layer, and forming a source/drain in said semiconductor layer and said other semiconductor layer in sandwiching relation to a region directly below said gate electrode.

[c17] 17. A method of manufacturing a semiconductor device having a gate electrode formed on a semiconductor layer with a gate insulating film interposed therebetween and a source/drain formed in the semiconductor layer, comprising the steps of:
forming a laminated region of a sacrificial layer and a semiconductor layer and a device separating region surrounding said laminated region, on a substrate;
forming a gate electrode on said device separating region and said semiconductor layer with a gate insulating film interposed therebetween;
forming a source/drain in said semiconductor layer in sandwiching relation to a region directly below said gate electrode;
forming an interlayer insulating film on the entire surface;

forming a contact hole extending through said interlayer insulating film; and

removing said sacrificial layer through said contact hole to form a cavity below said semiconductor layer.

[c18] 18. The method according to claim 17, wherein said step of forming the contact hole extending through said interlayer insulating film comprises the step of forming the contact hole extending through said interlayer insulating film to said sacrificial layer, further comprising the step of:

after said step of removing said sacrificial layer through said contact hole, forming an impurity diffusion layer in a region directly below said contact hole.

[c19] 19. The method according to claim 17, further comprising the steps of:

after said step of the source/drain in said semiconductor layer, silicidizing said source/drain entirely, wherein said interlayer insulating film is formed on the entire surface after said step of silicidizing said source/drain entirely;

wherein said step of forming the contact hole comprises the step of forming the contact hole extending through said interlayer insulating film to said silicidized source/drain; and

wherein said step of removing said sacrificial layer through said contact hole to form said cavity below said

semiconductor layer comprises the step of removing said sacrificial layer through said contact hole and said silicidized source/drain to form said cavity below said semiconductor layer.

[c20] 20. The method according to claim 17, further comprising the step of:
after said step of removing said sacrificial layer through said contact hole to form said cavity below said semiconductor layer, processing a surface of said substrate according to wet etching.

[c21] 21. A semiconductor device having a gate electrode formed on a semiconductor layer with a gate insulating film interposed therebetween and a source/drain formed in the semiconductor layer, comprising:
a dome-shaped semiconductor disposed on a substrate;
a gate insulating film and a gate electrode disposed on an outer wall surface of said dome-shaped semiconductor; and
a semiconductor layer disposed on an inner wall surface of said dome-shaped semiconductor and having a source/drain formed therein in sandwiching relation to a region directly below said gate electrode.

[c22] 22. A method of manufacturing a semiconductor device having a gate electrode formed on a semiconductor layer

with a gate insulating film interposed therebetween and a source/drain formed in the semiconductor layer, comprising the steps of:

forming a first semiconductor layer partly on a surface of a substrate;

forming a second semiconductor layer on an entire surface;

forming a gate insulating film and a gate electrode on said second semiconductor layer directly above said first semiconductor layer;

forming an opening extending to said first semiconductor layer in said second semiconductor layer and selectively removing said first semiconductor layer thereby to form a dome-shaped semiconductor which comprises said second semiconductor layer; and

forming a third semiconductor layer on an inner wall surface of said dome-shaped semiconductor, with a source/drain formed in said third semiconductor layer.

[c23] 23. The method according to claim 22, wherein said step of forming the third semiconductor layer on the inner wall surface of said dome-shaped semiconductor comprises the steps of:

forming a fourth semiconductor layer serving as a cap layer on the inner wall surface of said dome-shaped semiconductor; and

thereafter, forming said third semiconductor layer on said fourth semiconductor layer.

[c24] 24. The method according to claim 22, further comprising the steps of:
after said step of forming the third semiconductor layer on the inner wall surface of said dome-shaped semiconductor, forming an insulating layer to fill an interior space of said dome-shaped semiconductor and cover an outer surface of said dome-shaped semiconductor; and
etching said insulating film to form a BOX layer to fill a space between said substrate and said third semiconductor layer and also to form a side wall of said gate electrode.

[c25] 25. A method of manufacturing a semiconductor device having a dome-shaped semiconductor, comprising the steps of:
forming a first semiconductor layer partly on a surface of a substrate;
forming a second semiconductor layer on an entire surface; and
forming an opening extending to said first semiconductor layer in said second semiconductor layer and selectively removing said first semiconductor layer thereby to form a dome-shaped semiconductor which comprises said second semiconductor layer.